What is claimed is:

1. A fin field-effect transistor comprising:

a substrate;

a fin above the substrate;

a drain region and a source region outside the fin above the substrate;

a gate which extends essentially along the entire height of at least a part of the fin; and

a first diffusion barrier arranged between each of the drain region and the fin and the source region and the fin,

wherein the fin acts as a channel between the source region and the drain region.

2. The fin field-effect transistor according to Claim 1, in which at least one of the drain region and the source region include a polysilicon.

3. The fin field-effect transistor according to Claim 1, wherein:

the drain region and the source region are formed from a material with metallic conductivity, and

a Schottky barrier is formed between the drain region and the fin and between the source region and the fin.

4. The fin field-effect transistor according to Claim 3, wherein the material with metallic conductivity comprises at least one a platinum silicide, a platinum germanium silicide, and an erbium silicide.

5. The fin field-effect transistor according to Claim 1, wherein the substrate includes silicon oxide.

6. The fin field-effect transistor according to Claim 1, wherein the fin includes silicon.

7. The fin field-effect transistor according to Claim 1, wherein the source region is arranged at one end of the fin and the drain region is arranged at another end of the fin.

8. The fin field-effect transistor according to Claim 7, wherein:

two end faces terminate the fin in its longitudinal extent,

the source region at one end face of the fin cooperates with the fin, and

the drain region at the other end face of the fin cooperates with the fin.

9. The fin field effect transistor according to Claim 8, wherein:

two broad sides connect the end faces of the fin,

the source region cooperates with the fin with a part, not covered by a gate, of the broad sides of the fin, and

the drain region cooperates with the fin with a further part, not covered by the gate, of the broad sides of the fin.

10. The fin field-effect transistor according to Claim 8, wherein:

the source region cooperates with the fin exclusively at one end face of the fin, and

the drain region cooperates with the fin exclusively at the other end face of the fin.

11. The fin field-effect transistor according to Claim 1, comprising a spacer at least above a part of the fin.

12. The fin field-effect transistor according to Claim 11, wherein the spacer extends essentially along the entire height of the part of the fin.

13. The fin field-effect transistor according to Claim 11, wherein:

the gate is arranged between two spacers, and

a protective layer is arranged above the gate.

14. The fin field-effect transistor according to Claim 11, wherein the spacer and the protective layer include at least one of a silicon oxide and a silicon nitride.

15. The fin field-effect transistor according to Claim 11, wherein the gate extends along the entire length of the fin, and the outer sides of the spacers lie in one plane with the end faces of the fin.

16. The fin field-effect transistor according to Claim 1, comprising an insulation layer at least partially bounding the source region and the drain region is provided, wherein the drain and source regions have a smaller height above the substrate surface than the insulating region.

17. A method for fabricating a fin field-effect transistor, comprising:

forming a fin above a substrate;

forming a gate layer at least above a part of the fin;

applying an insulation layer after forming the gate layer;

removing the insulation layer in relation to the ends of the fin so that at least a part of the ends of the fin is uncovered; and

filling, at least partly, the regions uncovered from the insulating layer with material for forming a source region and a drain region.

18. The method for fabricating a fin field-effect transistor according to Claim 17, wherein the fin is formed above the substrate by:

applying a mask for structuring of a fin to one silicon layer of two silicon layers enclosing a basic oxide layer; and

removing the silicon material of the one silicon layer so that a silicon body in the form of the fin is formed on the basic oxide layer.

19. The method for fabricating a fin field-effect transistor according to Claim 18, wherein the mask contains at least one of a silicon oxide and a silicon nitride.

20. The method for fabricating a fin field-effect transistor according to Claim 17, wherein the gate is formed above the fin by:

applying a gate layer;

applying a protective layer to the gate layer;

applying a mask for the further structuring of the gate; and

removing excess material of the gate and protective layers so that a strip-shaped stack, laid over the fin, made from the gate layer and the protective layer is formed.

21. The method for fabricating a fin field-effect transistor according to Claim 20, wherein spacers are formed by:

coating the arrangement with a spacer layer; and

removing the spacer layer so that the spacer layer forms spacers at least on the sides of the gate that are still uncovered before the coating with the spacer layer.

22. The method for fabricating a fin field-effect transistor according to Claim 21, wherein

the outer sides of the spacers arranged on the side of the gate lie in one plane with the end faces of the fin, and

a diffusion barrier is arranged on each uncovered end face of the fin before the application of the insulation layer.

23. The method for fabricating a fin field-effect transistor according to Claim 20, wherein at least one of the spacer layer and the protective layer contains silicon nitride.

24. The method for fabricating a fin field-effect transistor according to Claim 17, wherein the insulation layer is removed in the region of the ends of the fin after a masking operation marking the regions to be uncovered.

25. The method for fabricating a fin field-effect transistor according to Claim 17, wherein the material deposited for forming at least one of the source and the drain region is doped before or after it is deposited.